Amendments to the Claims:

A clean version of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121(c) (3). This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) A processor for executing digital signal processing under control of a clock facility, such that a sequence of **C** effective clock cycles will effect a processing operation of a predetermined amount of image information,

said processor being characterized in having programming means for implementing programmable stall clock cycles interspersed between said effective clock cycles for implementing a programmable slowdown factor **S**, such that a modified number of **C*S** overall clock cycles will effect processing of said predetermined amount of digital signal information.

2. (Original) A processor as claimed in Claim 1, and having said programming means controlling the interspersing in an at least substantially periodical manner.

3. (Original) A processor as claimed in Claim 1, effectively representing a coprocessor and having a control processor as said programming means.

4. (Original) A processor as claimed in Claim 3, wherein said coprocessor and said control processor are interconnected by a bus to a shared memory facility.

5. (Original) A processor as claimed in Claim 4, wherein said coprocessor, said control processor and said bus are disposed on a single semiconductor chip, whereas said shared memory facility is at least substantially off-chip.

6. (Currently Amended) A processor as claimed in Claim 1, and being arranged to execute at least two different image processing operations under ~~resepective~~ respective different percentages of stall clock cycles.

7. (Original) A processor as claimed in Claim 1, wherein said programming means drive an incrementable storage facility through a periodical increment by a number **N** that is a function of said factor **S** according to **N = round (R * x)** , wherein **x = (S - 1 / S)** and **R** is the range of the storage facility, and wherein a carry output signal of the storage facility will generate an effective clock cycle.

8. (Original) A processor as claimed in Claim 5, wherein at least one other bus station than the coprocessor is arranged and allowed to temporarily grab the bus in an interval during a said stall cycle.